Developing 3-D Imaging Sensors

Problems and Technologies

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Outline

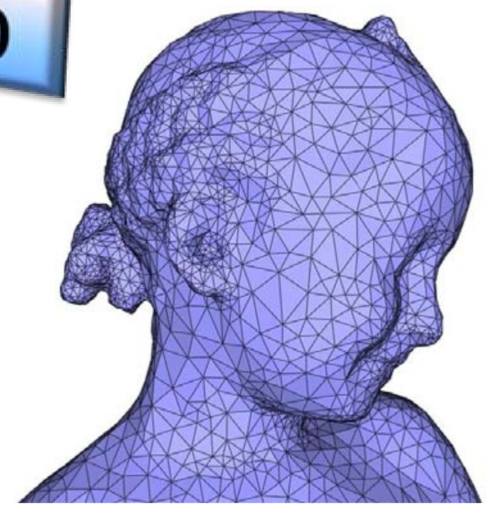
- outlook to 3D applications
- time-of-flight measuring technique
- comparing PULSED and SWM approaches
- developing the Photo-demodulator in CMOS
- measurements and conclusions

3-D Imaging

Today's technology is ready to develop photodetectors for the three-dimensional world !!

2D

3D



adding distance information

pixels describe the intensity pattern I(x,y)

pixels describe morphology z(x,y)

typical applications

- Homeland security
- Navigation aids
- Virtual reality
- Robotics
- Cultural heritage
- Ambient assisted living

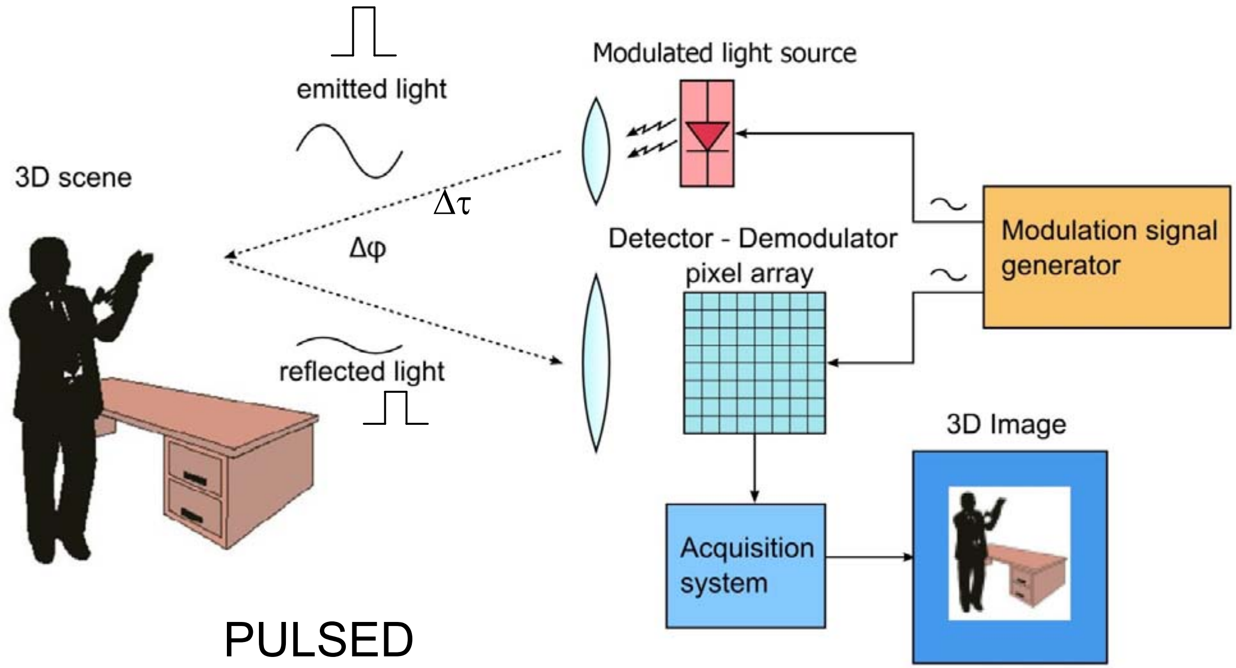





techniques for 3D imaging

- Triangulation
  - bulky, requires scanning
  - short distance
  - medium/low resolution
- Interferometry
  - very high resolution
  - expensive, critical to operate
- **Time-of-flight** (pulsed or SWM) →
  - Compact, may be scannerless
  - Fast acquisition
  - Large distance range
  - Cost-effective
  - Active (illuminator required)
  - Ambiguity range limitation

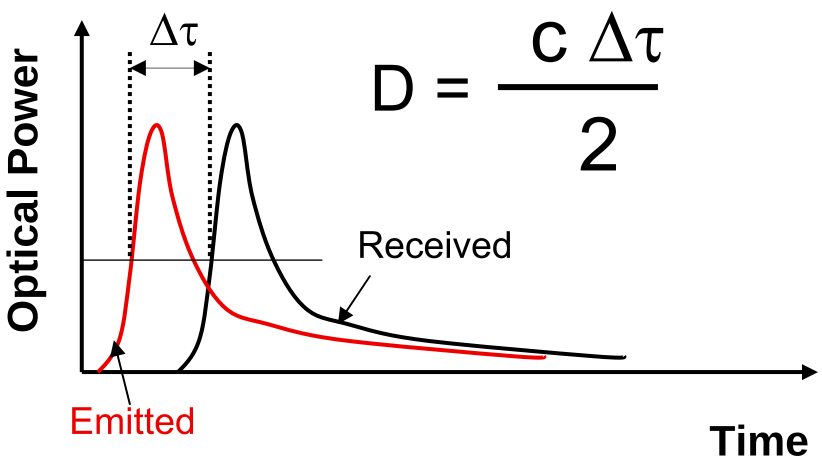
Time-of-Flight rangefinders



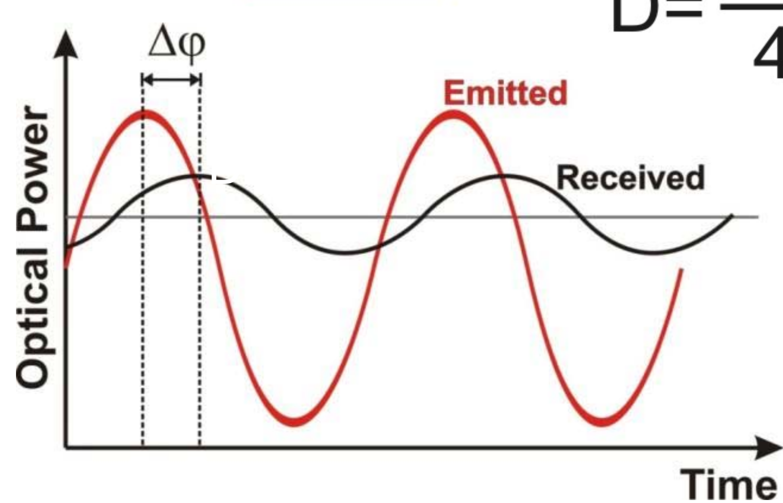
SW (sine wave) Modulated

$$D = \frac{c\,\Delta\varphi}{4\pi f_m}$$

PULSED



$$D = \frac{c\,\Delta\tau}{2}$$

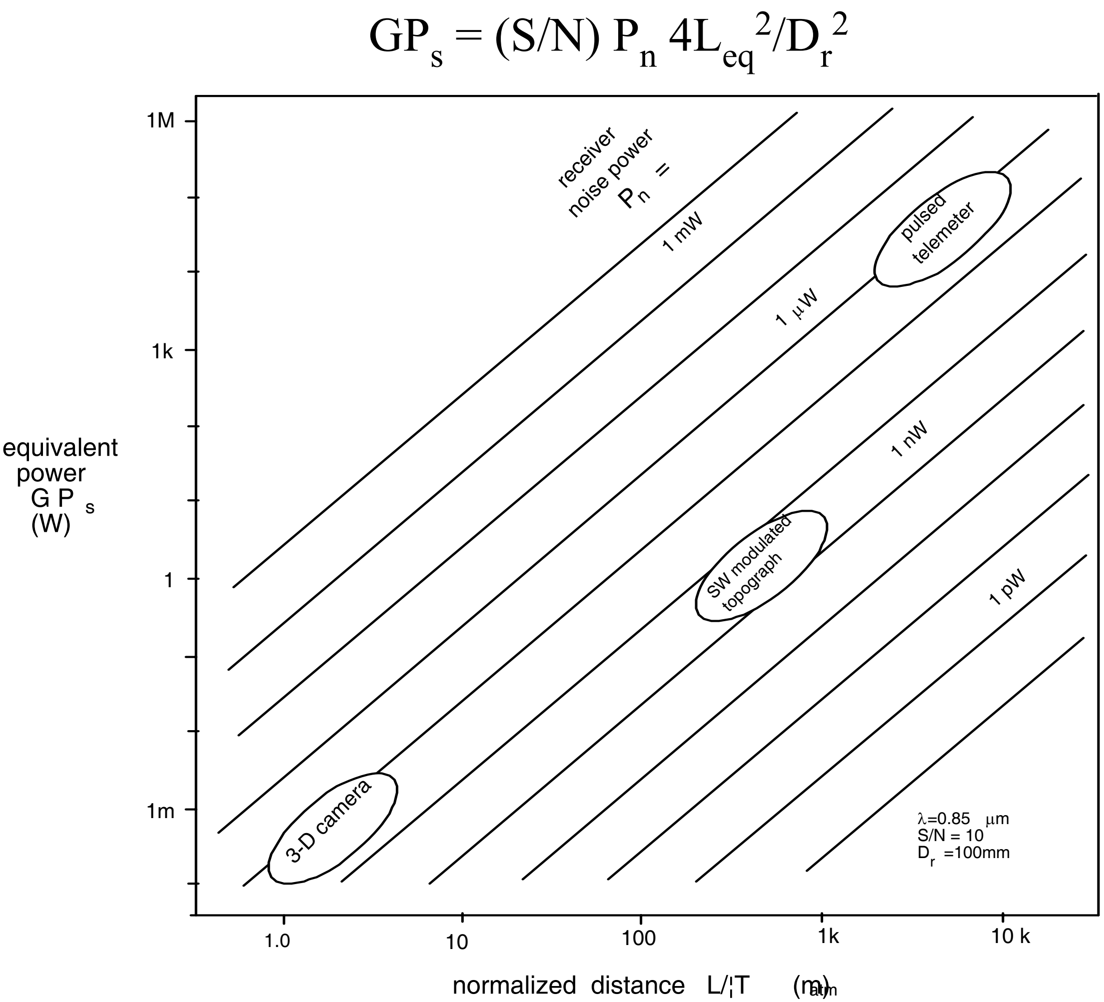


in most applications, to be interesting…

both PULSED and SW 3-D developments should entail:

- integration of time-of-flight pixel on-board technology with the Silicon CMOS industry standard (and … *low-cost* !!) technology
- minimum invasiveness (optical power) of the active illumination required

analyzing Time-of-Flight rangefinders: pulsed vs SWM



theoretically equivalent at the quantum limit at equal average power, but PULSED is less sensitive to stray light, has some safety issues and requires more bandwidth to circuits. SW-modulated is short-distance, is about eyesafe, but has range ambiguity to circumvent

other features of PULSED and SW

- Pulsed 3-D requires a fast (sub-ns) detector for operation on short distances, and very fast time sorters to measure the ns-range time delay → *SPADs and Counters with TAC*

-this makes the pixel large and fill-factor low, requiring a lens-array for sensitivity recovery

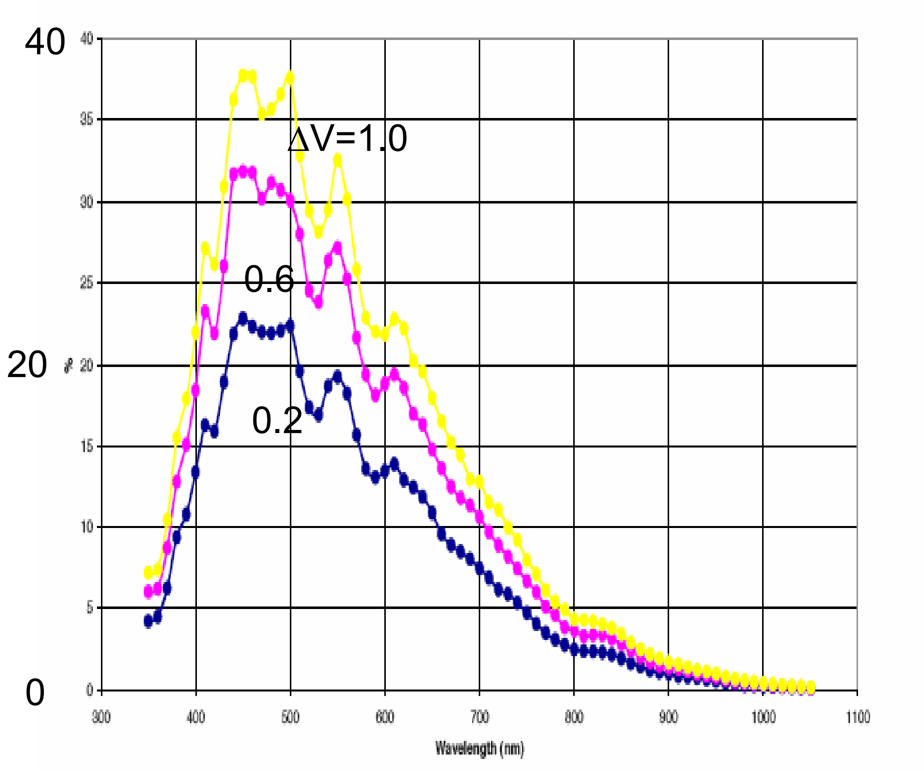
- SW works on moderate frequency (20 to 100 MHz) for 3-D short range, and by incorporating a demodulator into the detector → circuits are greatly simplified, and fill-factor is high

detour on the PULSED 3-D approach

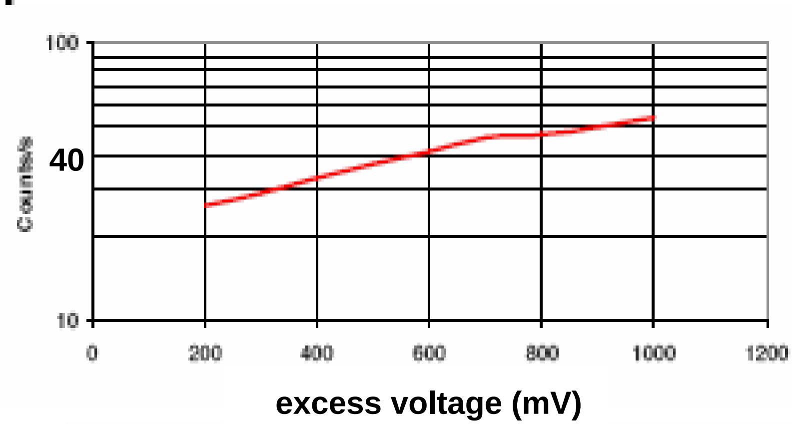
- in 3-D, PULSED is a competitor to SWM but calls for a fast (sub-ns) detector able to resolve the sub-ns propagation times of short-range applications
- the SPAD (Single Photon Avalanche Detector) is the suitable choice of photosensor
- SPAD is compatible to fine CMOS technology
- an *FET-STREP European Program* pursued development of a 120-nm CMOS 3-D and fast spectroscopy imaging (32x32 and 128x160 pixels) device – the *MEGAFRAME* project

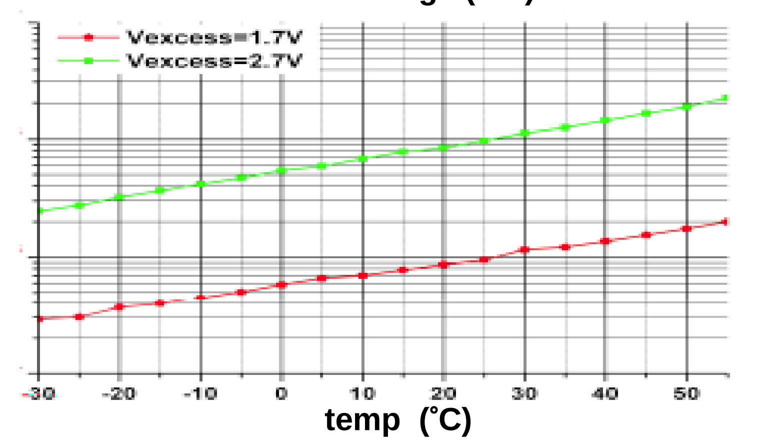
CMOS SPAD parameters

a 50 μm active diameter devices has been designed in 120-nm CMOS with good performances of:



high probability of detection
(35%@1-V overdrive)

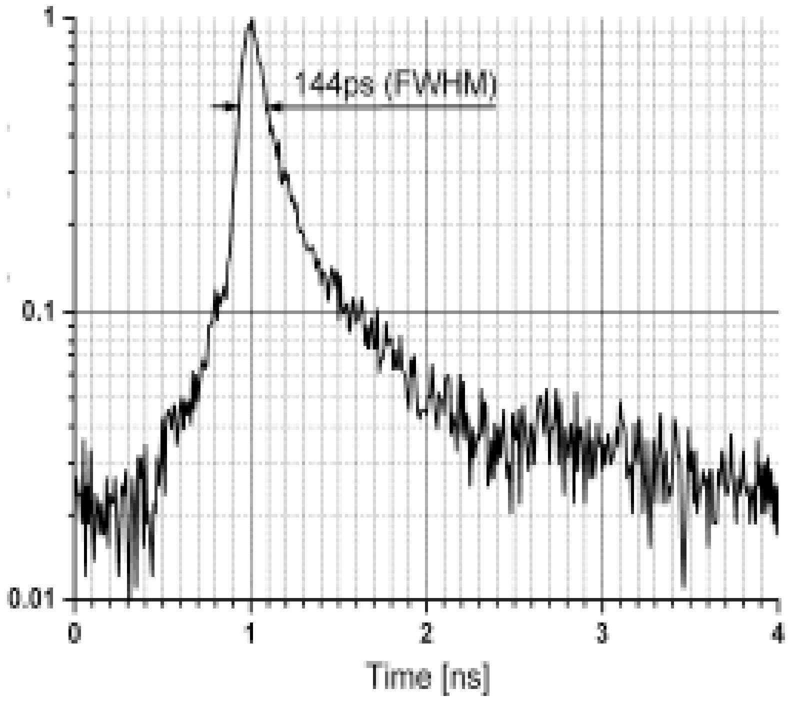




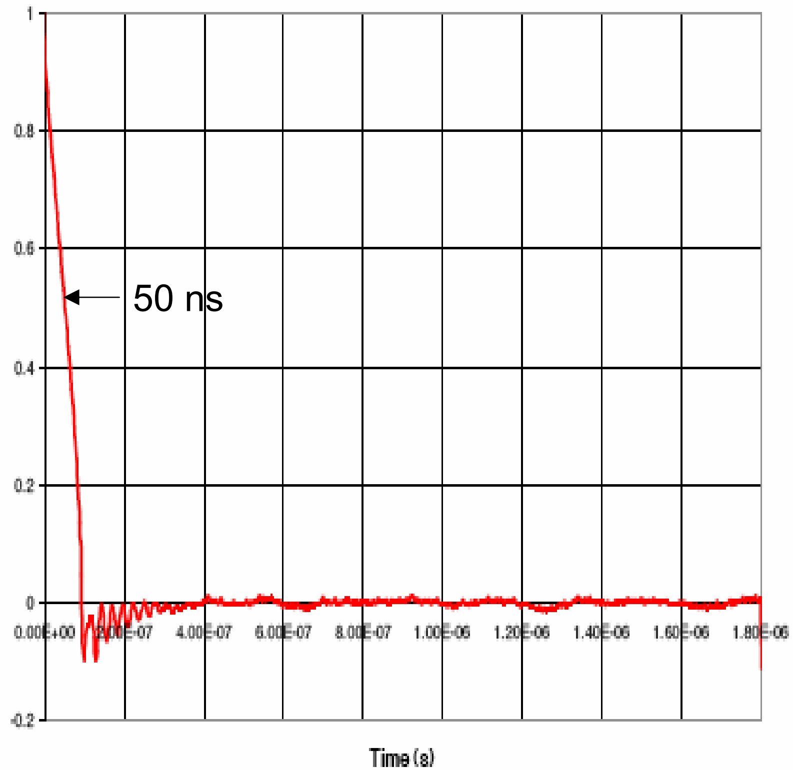
low dark counts rate
(40 Hz for a 6-μm dia.)

CMOS SPAD parameters II

and, not less important:



sub-ns time resolution
(61 ps rms)



low afterpulsing
(negligible @ T_{ho}>200ns)

On-board pixel processing

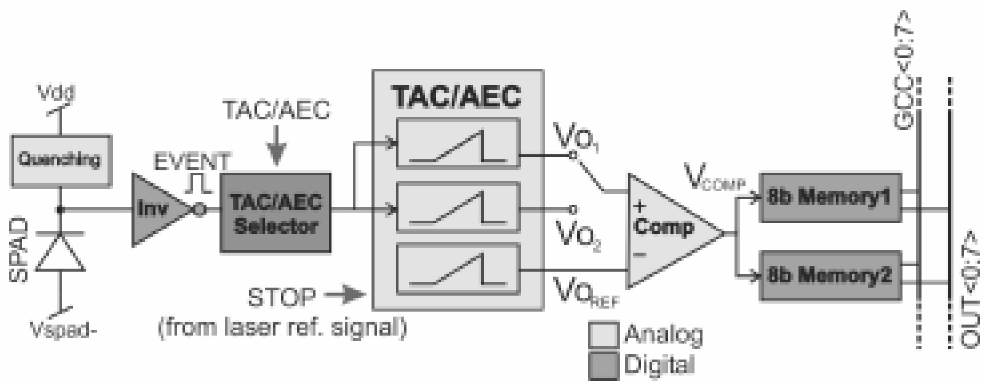


Figure 1. Pixel block diagram.

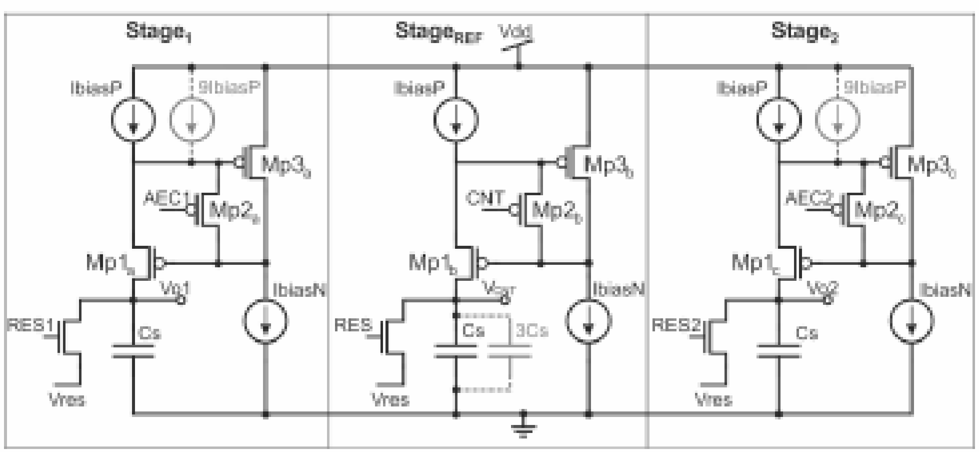


Figure 2. Circuit schematic of the TAC/AEC stage.

processing circuits implemented by CMOS technology in a 50-μm dia. pixel area around the 6-μm SPAD:

-active quenching

- premaplifier

- TAC

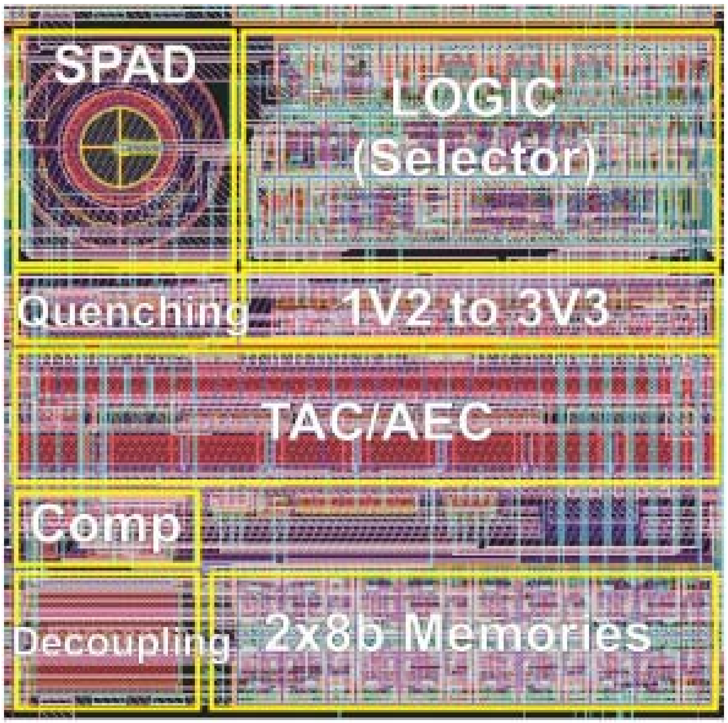
-comparator

-8-bit memory

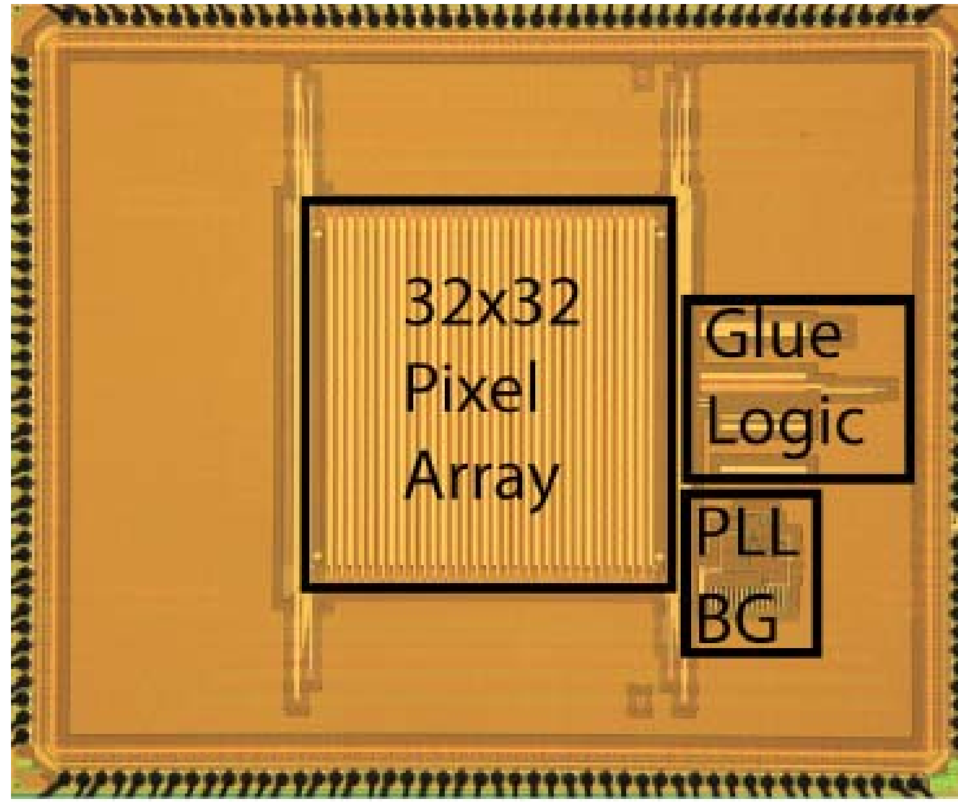
Stoppa et al.: ESSCIRC 2009

the CMOS SPAD pixel…

the pixel, 50-μm by side



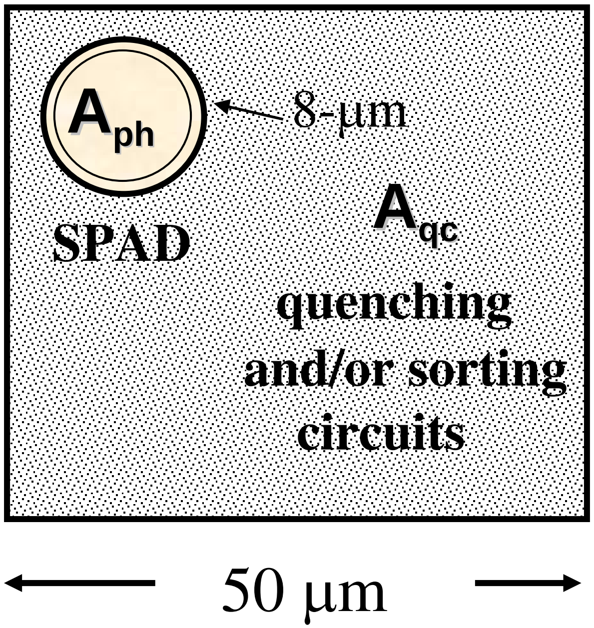
$FF = A_{ph}/(A_{qc}+A_{ph})$
(~ 0.02 in example above)



…and the 32x32 array chip, 4-mm by side

Stoppa et al.: ESSCIRC 2009

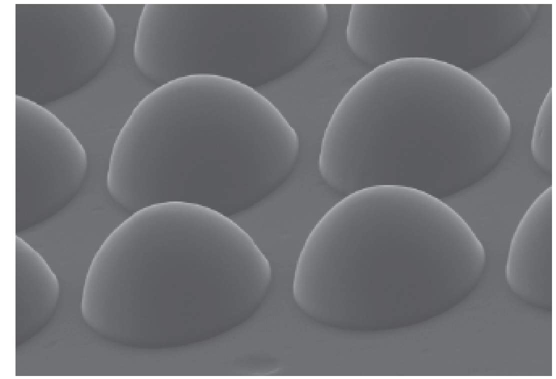
fill-factor recovery in SPAD

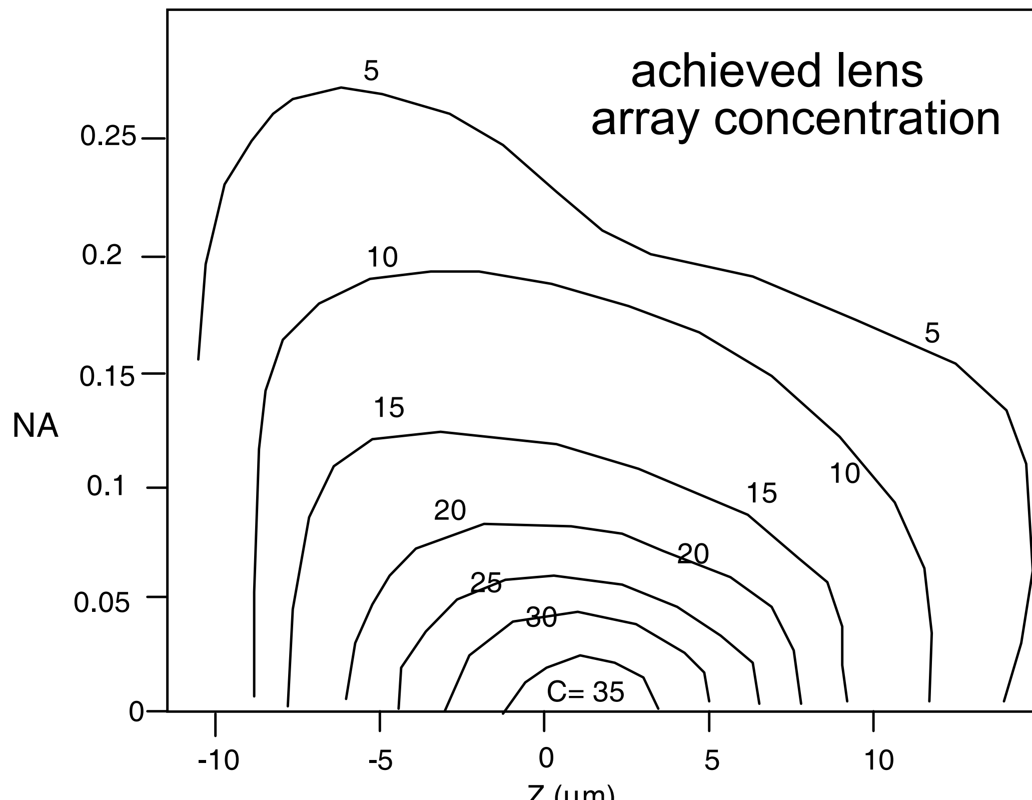


$FF = A_{ph}/(A_{qc}+A_{ph})$

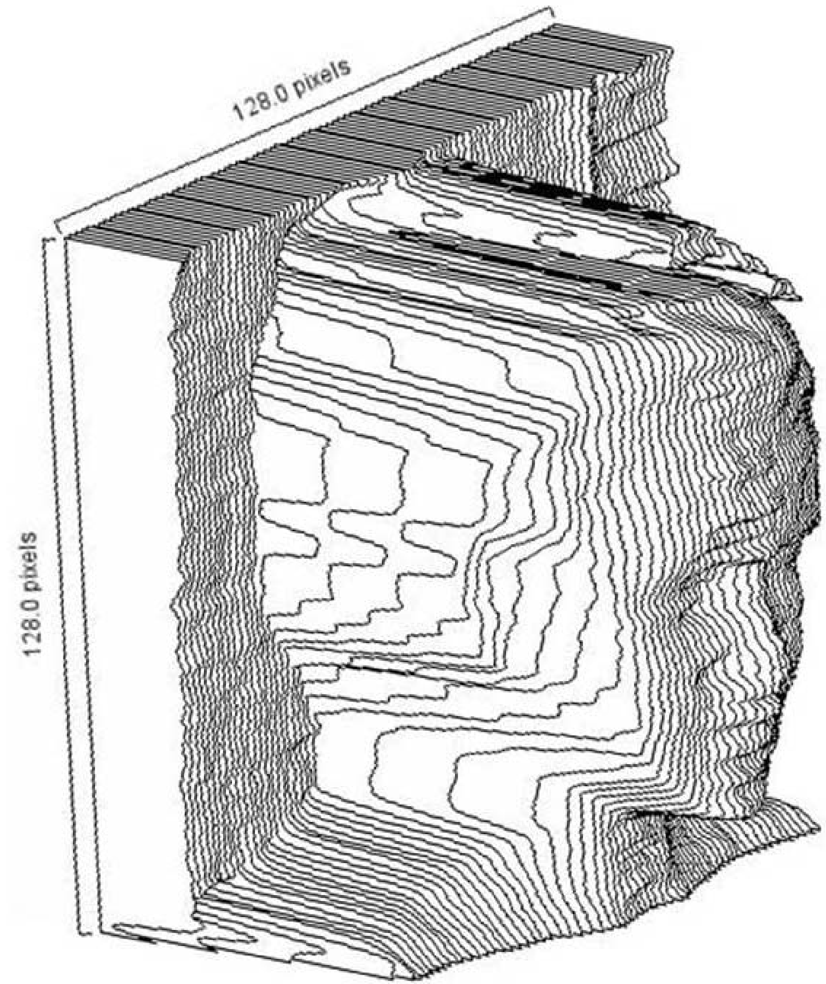
~ 0.02 in example above

then we use a 50-µm dia. lens-array to concentrate incoming optical power





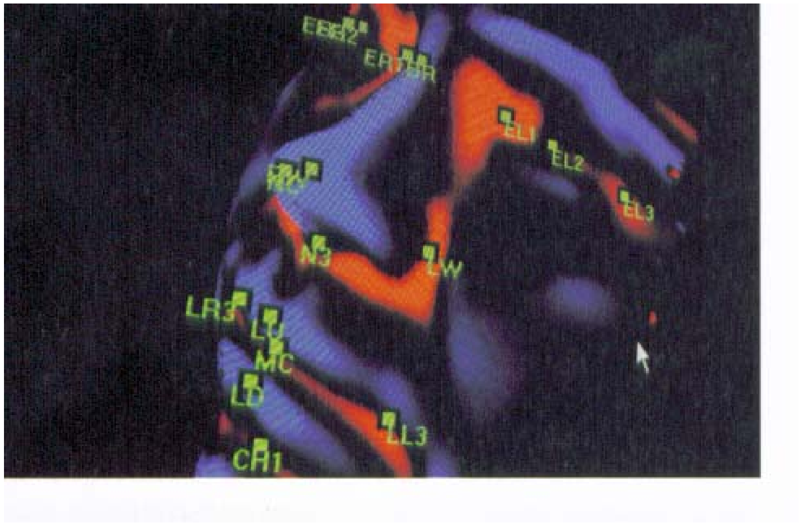
Example of 3D image pickup with the 32x32 SPAD array



Accuracy:
- **1mm (100 frames)**

Frame rate:
- **1Hz**

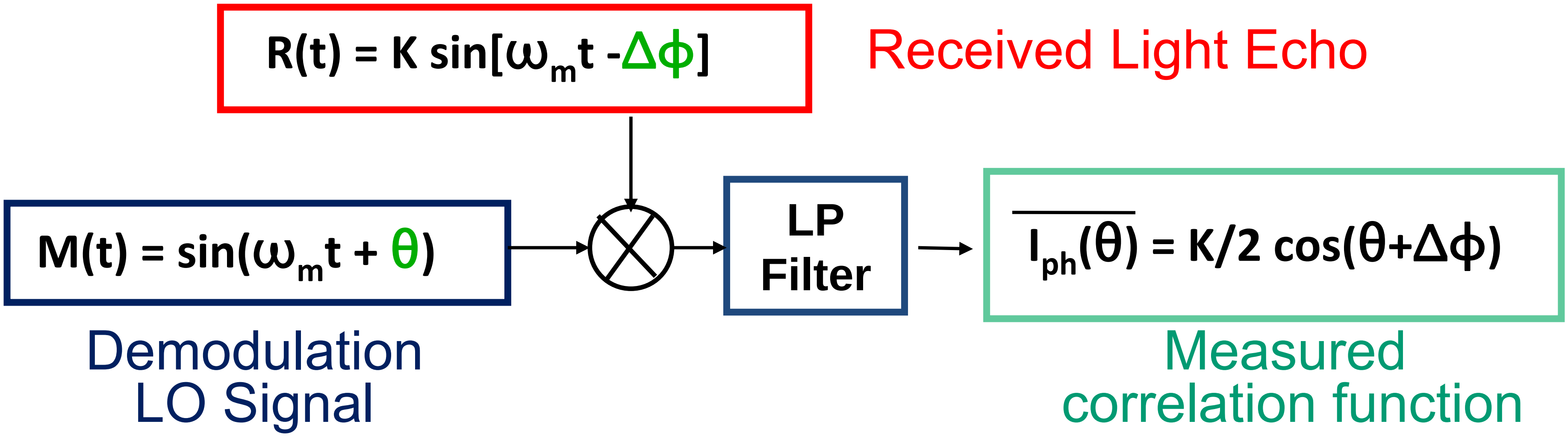
8-bit digital output



going back to SW-modulated…

- the SWM is attractive for 3-D if we can simplify data analogue processing
- then, we are asked to devise a high-efficiency photodetector, working with shallow epi-layer of a CMOS, low cost, standard industry process.
- the answer has been a specially designed, CMOS-compatible, high FF, photodetector demodulator

principle of SWM telemeter



recovery of phase $\Delta\phi$ amenable to CMOS integration of the pixel: the detected demodulation signal $I_{ph}(t)$ is sampled on 4-phases θ periods of the local oscillator M(t) so as to supply $I_1 = I_{ph}(\theta=0°)$, $I_2 = I_{ph}(\theta=90°)$, $I_3 = I_{ph}(\theta=180°)$, $I_4 = I_{ph}(\theta=270°)$, then we compute

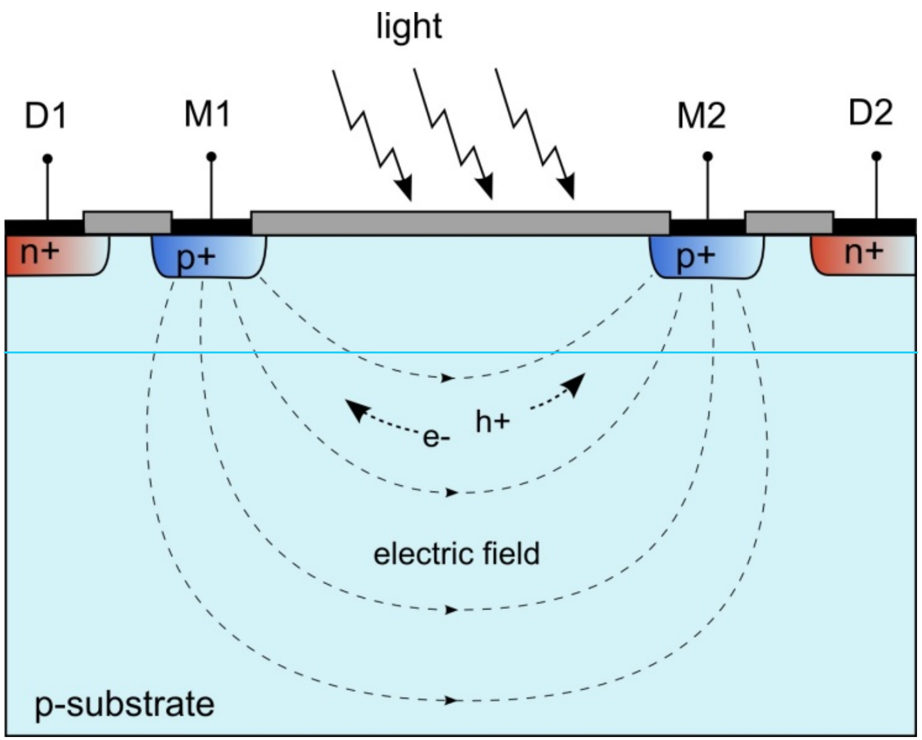
$$\Delta\varphi = \arctan\left(\frac{I_4 - I_2}{I_3 - I_1}\right)$$

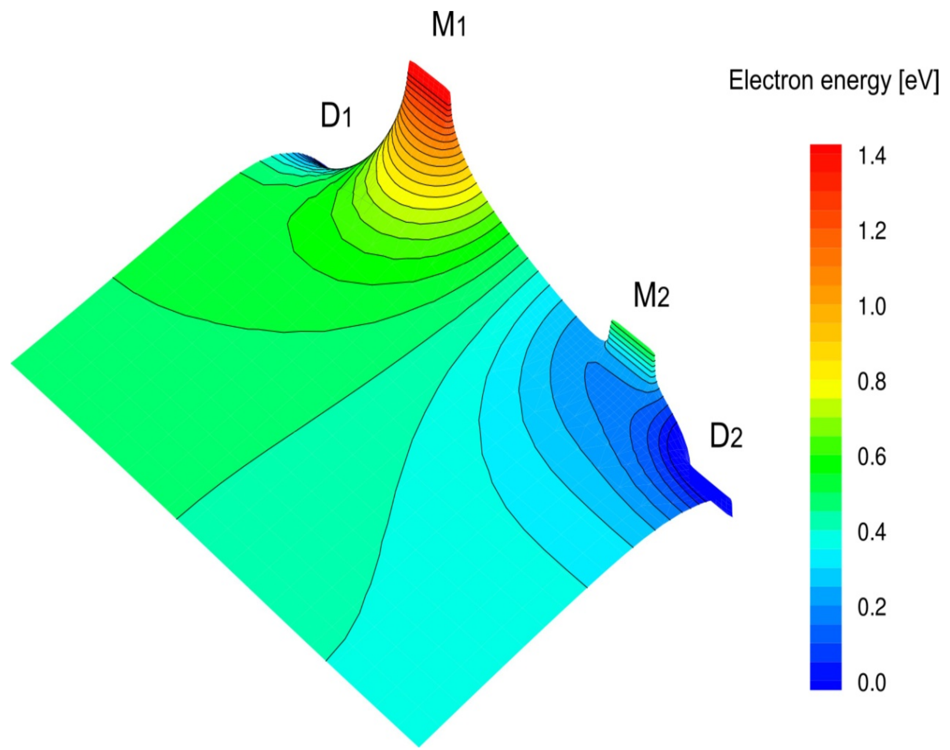
let's now have a look at

sensor architecture

- o design of a new photo-demodulator
- o pixel design
- o array architecture

PDD, the Photo-Demodulator Detector



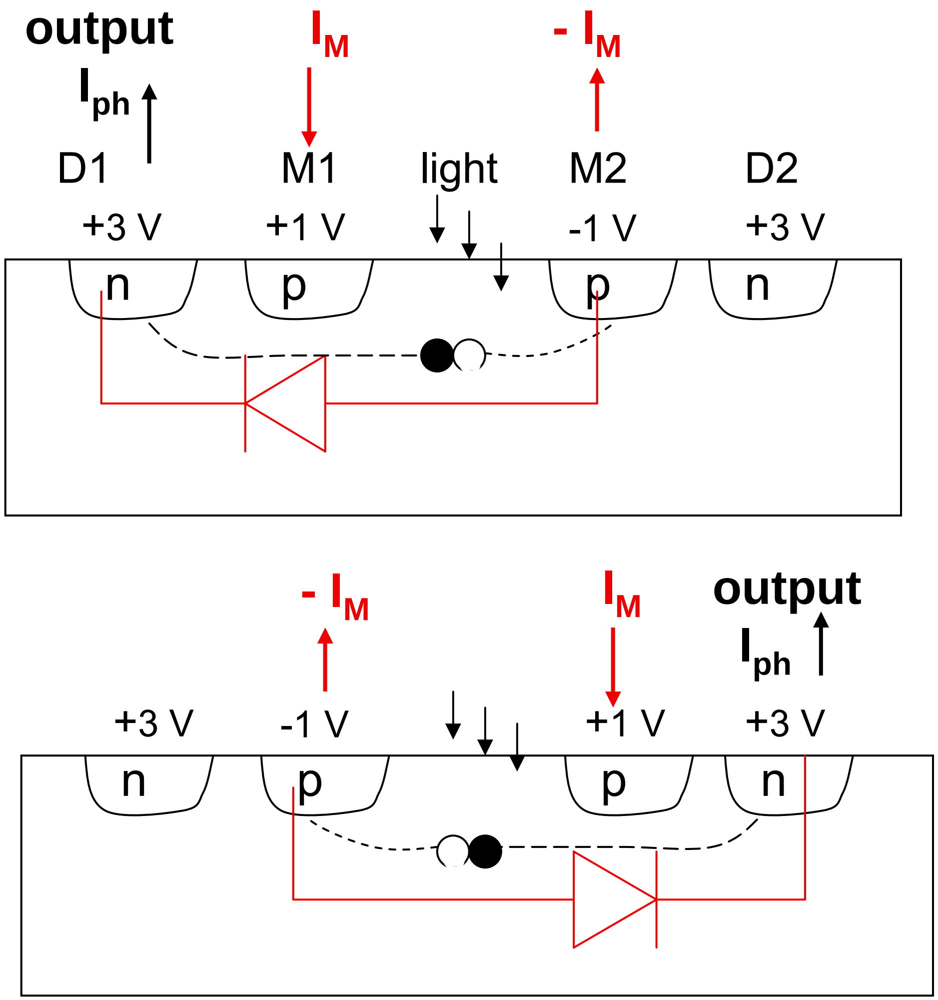


M1, M2: modulation electrodes

D1, D2: collection electrodes

first reported by: Van Nieuwenhove, et al., Proc. Symp. LEOS Benelux Chapter, 229-32 (2005)

more on the PDD



by pulsing a current I_M (50μA typ.) between electrodes M1 and M2, we can switch photocurrent I_{ph} from output D1 to output D2. If current I_M is a sine wave, process is a *demodulation* of the detected signal (wow!)

M1, M2: modulation electrodes, D1, D2: collection electrodes of the photo-demodulator detector (PDD)

features of PDD

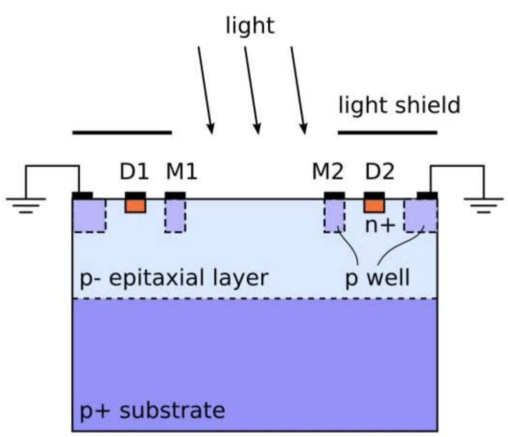
advantages:

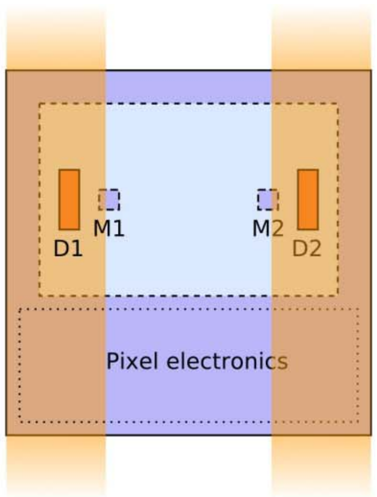
- High demodulation efficiency
- Fully Compatible with standard CMOS technology

issues:

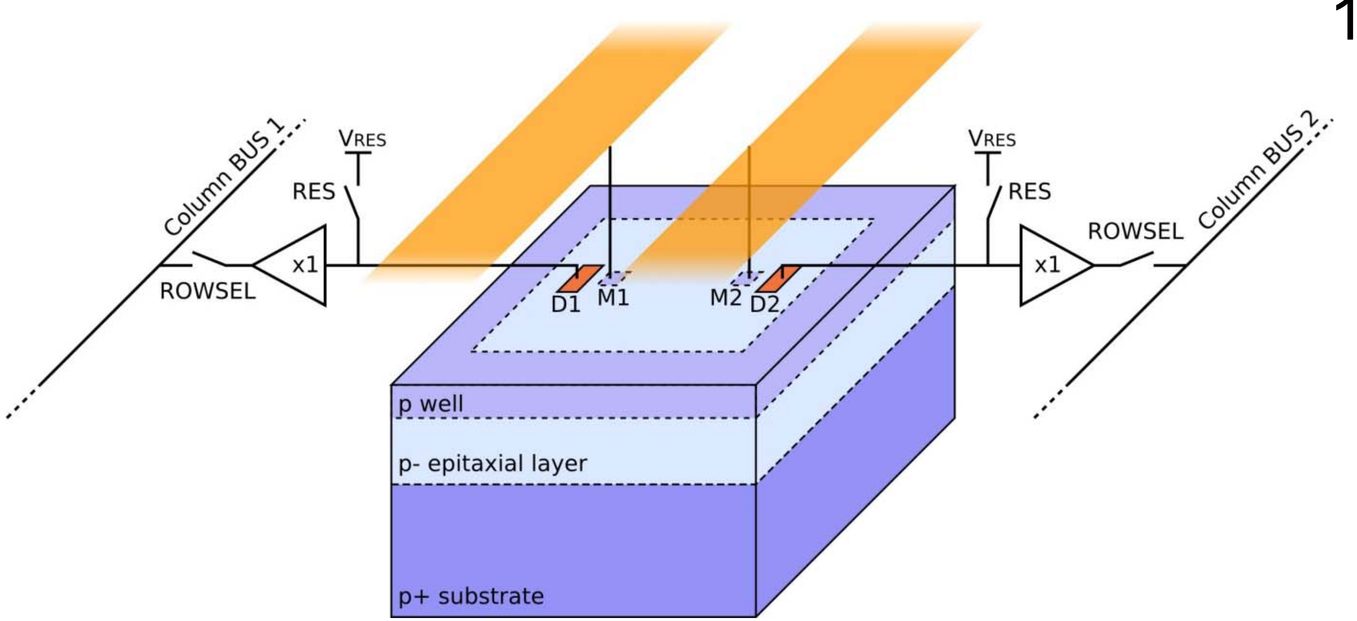
- High power consumption due to modulation current (about 100 mW)
- Pixel scalability questionable

Pixel Architecture

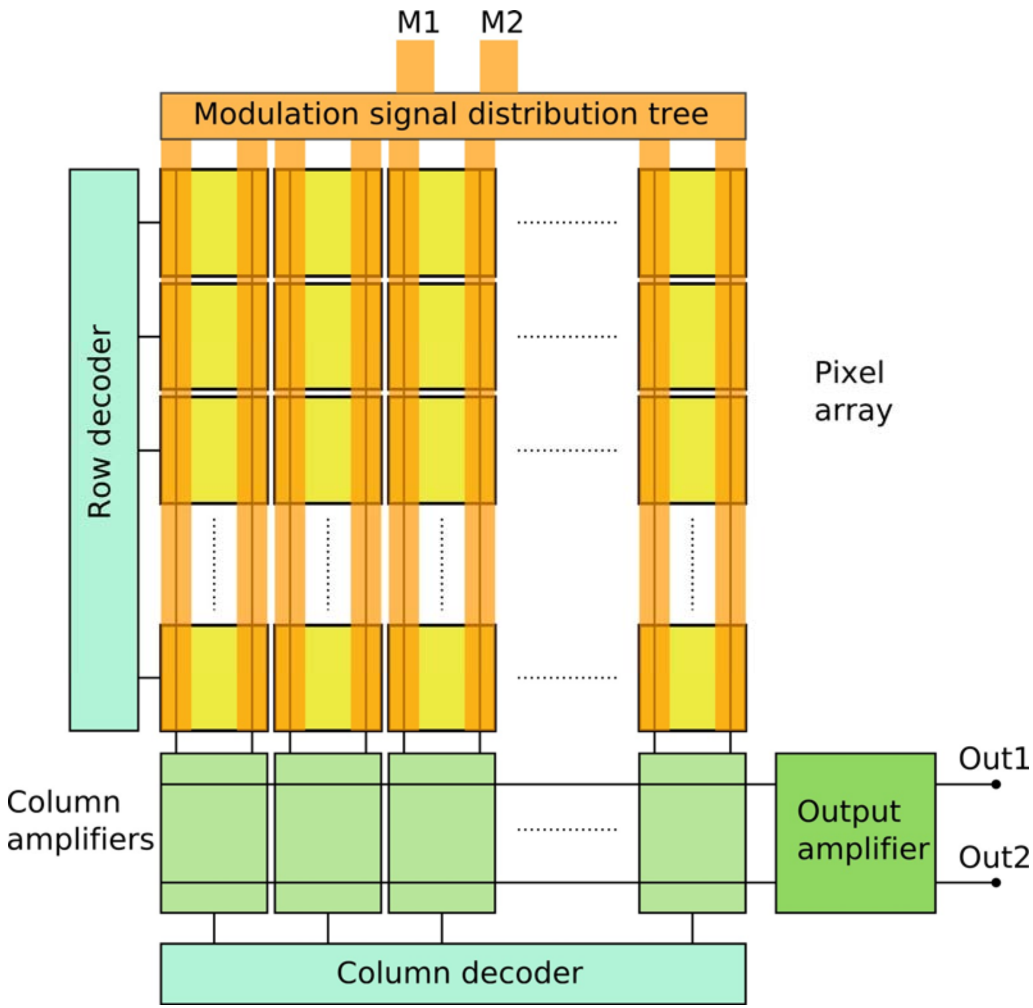




Technology:
180-nm CMOS
Pixel pitch: 10μm
Fill factor: 24%
1.8-V transistors

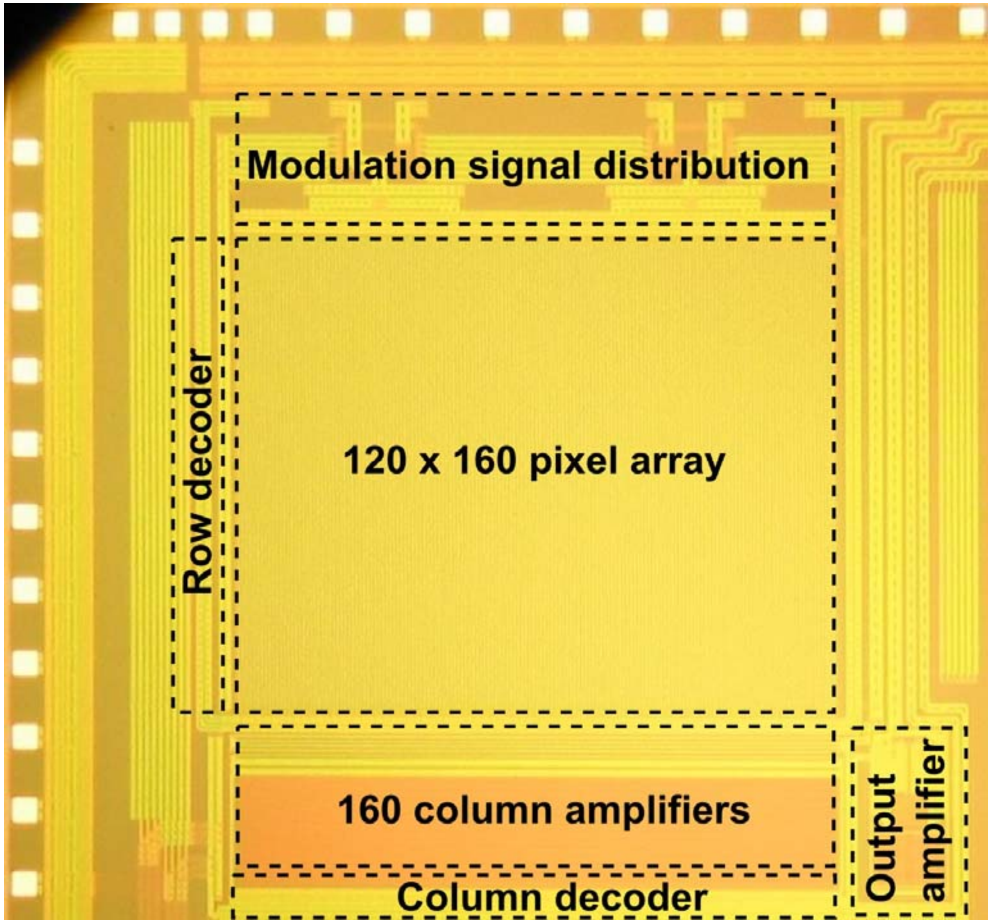


Sensor Architecture



- 120x160 pixel array
- Pseudo-differential pixel
- Column amplifiers
- Output DDS amplifier

Sensor Chip



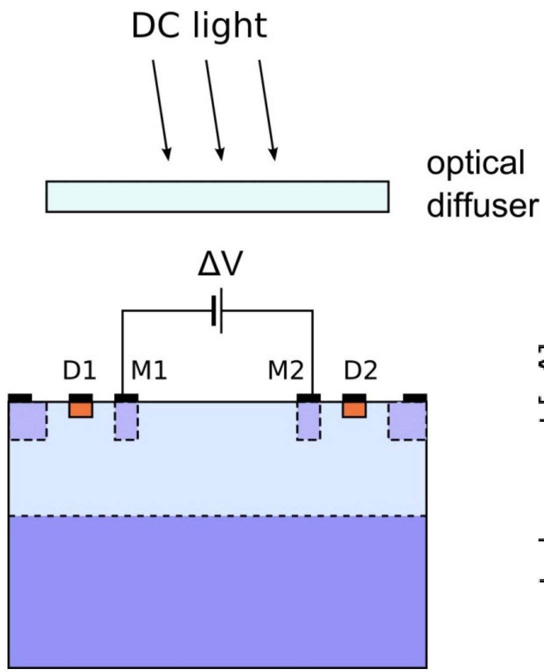
- CMOS 0.18μm 1P4M process
- Sensor area: **2.5**x**2.5**mm^2
- 1.8V and 3.3V transistors
- Epitaxial layer

  resistivity: 20 Ohm-cm

  thickness: 4μm

- Experimental Results:
  - o Photo-detector performance
  - o 3D imaging system

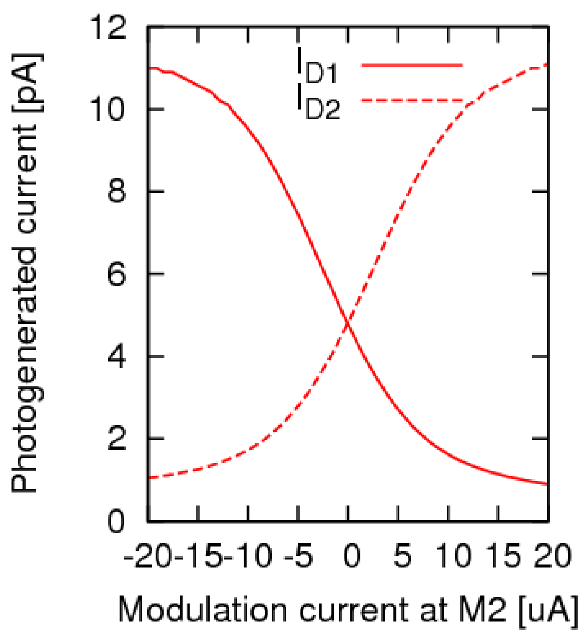
Photo-demodulator: DC Performance



R_{MOD} = 25 kOhm
dissipation 10 μW

DC demodulation contrast:

$$\chi = \frac{(I_{D1}-I_{D2})}{(I_{D1}+I_{D2})}$$



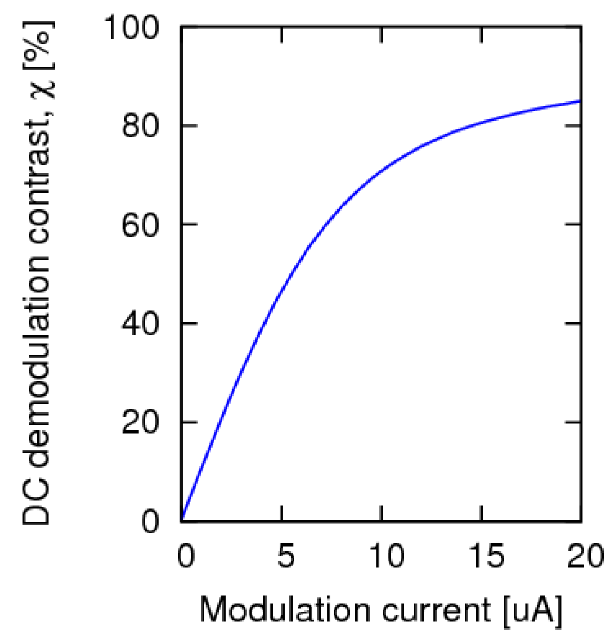
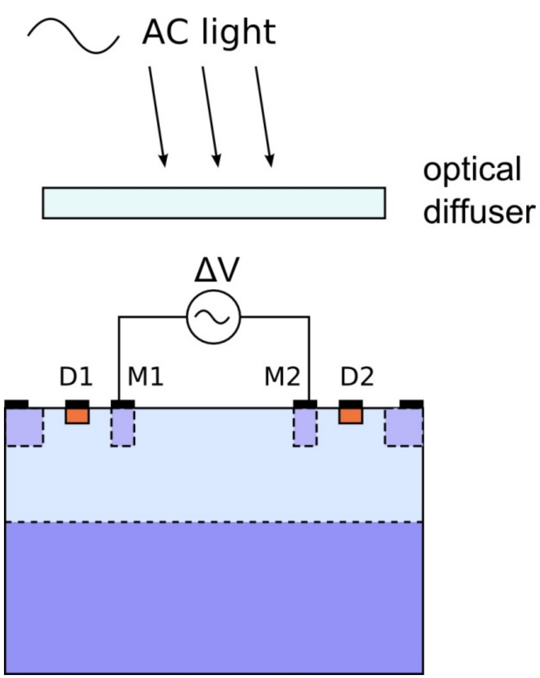


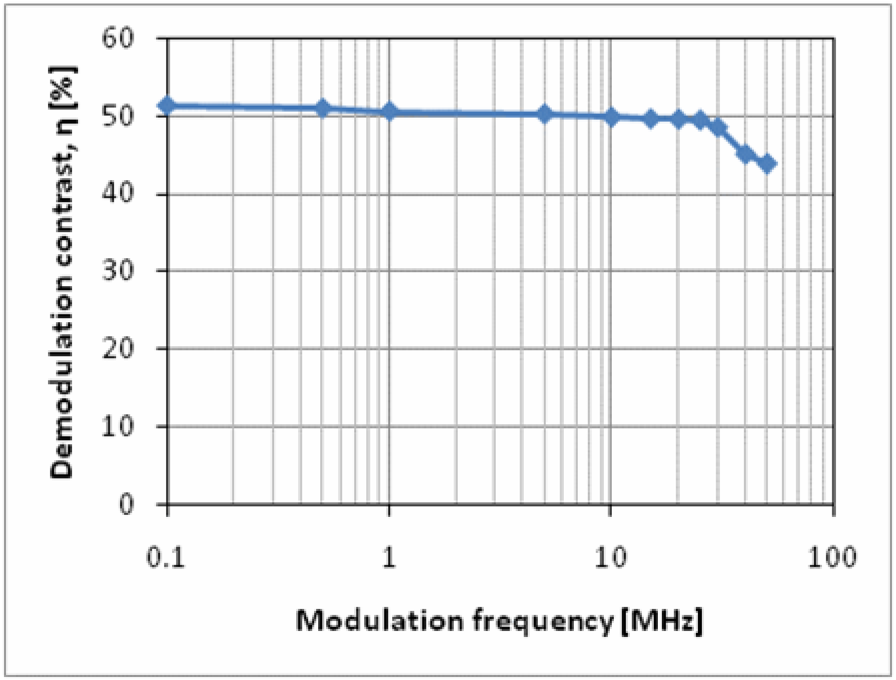
Photo-demodulator: AC Performance



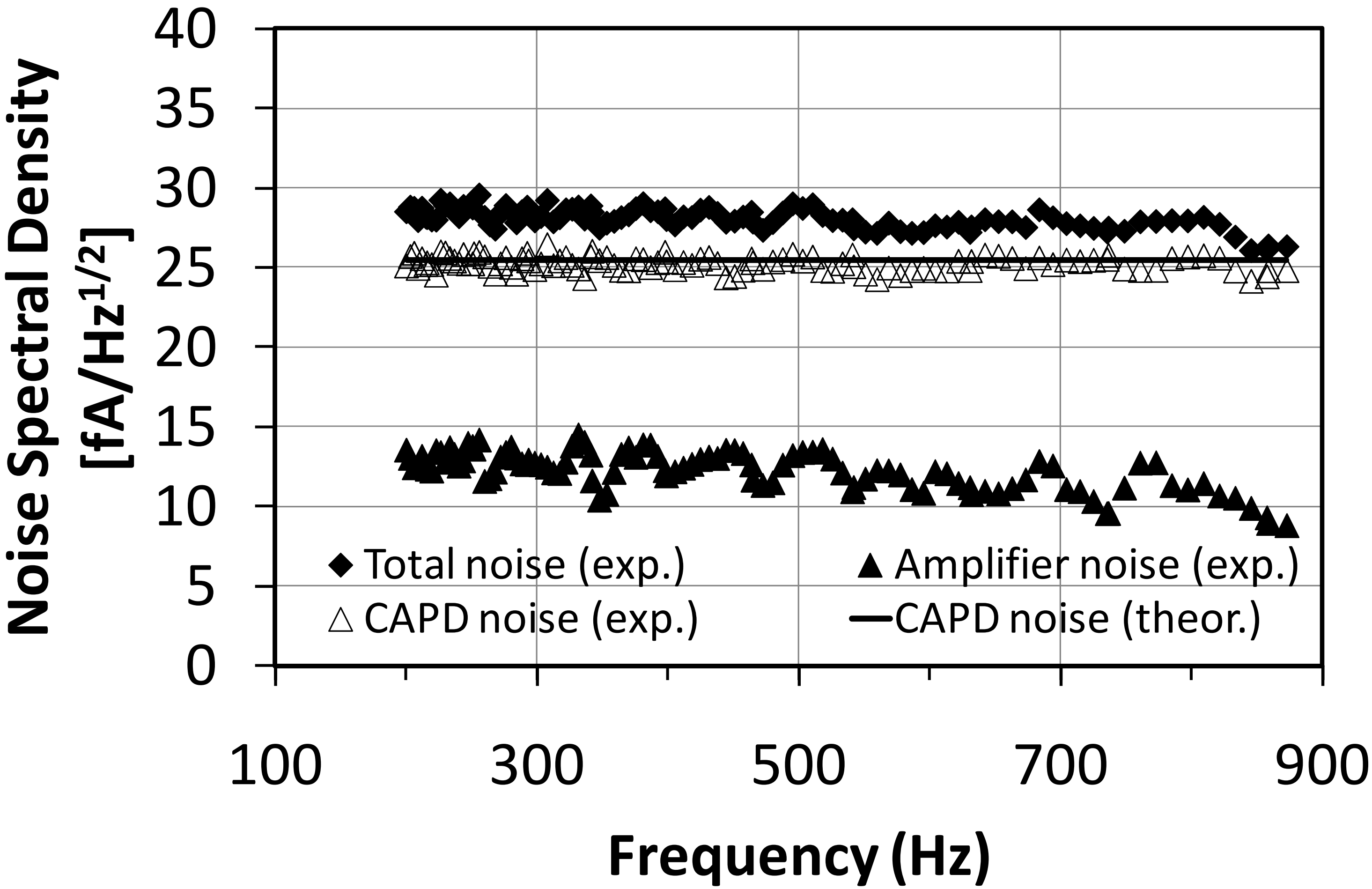
AC demodulation contrast:

$$\chi = \frac{(I_{D1}-I_{D2})_{max}}{(I_{D1}+I_{D2})}$$

Modulation current:16 µA/pixel (peak)



Noise Performance



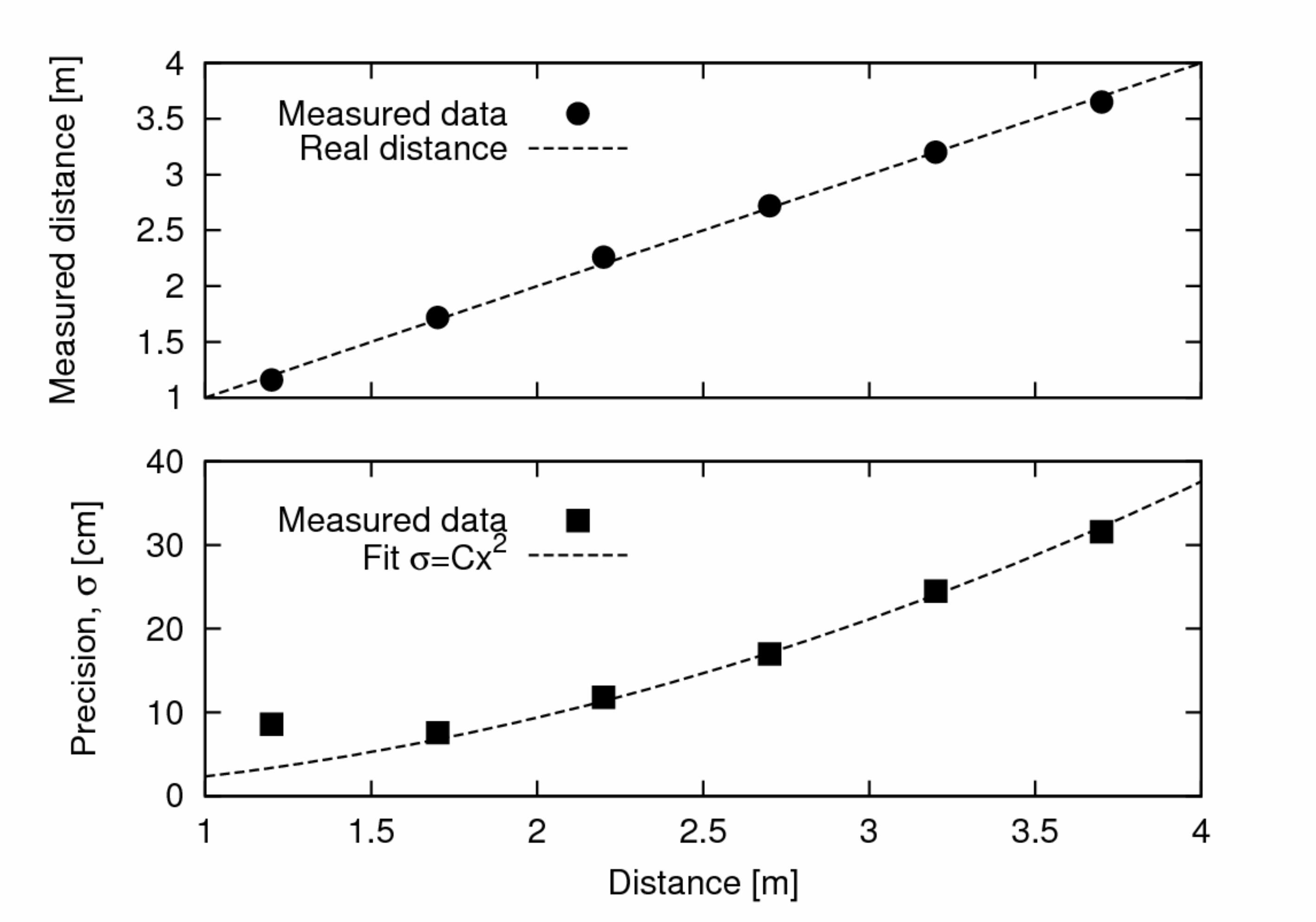
No appreciable excess noise is observed with respect to the shot-noise level ($I_{C1} \approx 2$ nA) due to the modulation resistance

3-D Imaging System

Illumination module:
- source: LED, 20 MHz, λ: 850nm
- power in the FoV: 140 mW
- class (IEC 60825-1): 1M

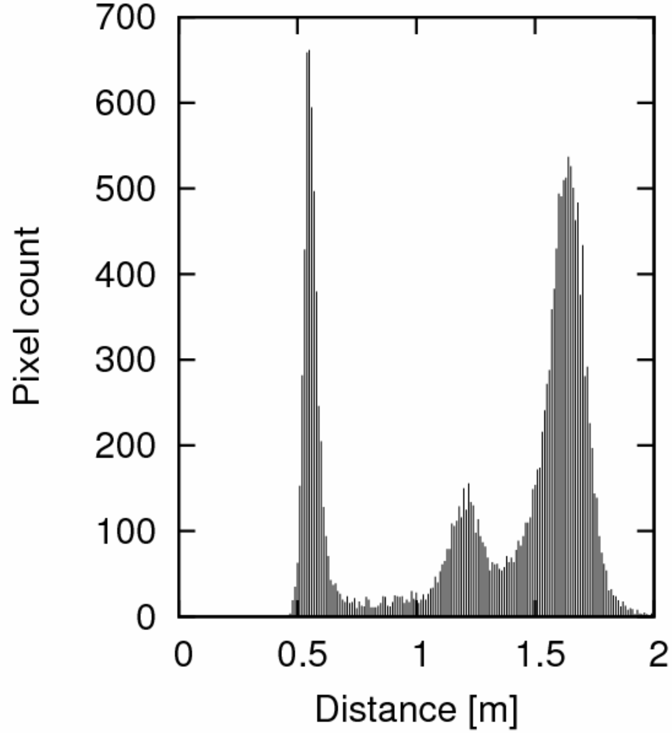
Sensor:
- objective 2.9-mm, F/1
- sensor FoV 23°x30°
- total modulaton current: 400 mA (peak)

Distance Measurement



Maximum non-linearity: 0.3%
Distance non uniformity among pixels: 0.2cm

3-D Image Example



Acquired with 400ms exposure time, 100 lux ambient light

in conclusion...

- Current Assisted Photo-Demodulator-Detector
  in CMOS technology demonstrated
- 10-μm, 24% fill-factor pixel achieved,
- 50% demodulation contrast at 20MHz and
- >50MHz cutoff frequency
- 120x160 3-D image sensor designed
- real-time 3-D Imaging demonstrated,
- then…

…the SWM CMOS 3-D approach is viable !....

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謝謝

thank you